

THOMAS W. FRY

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EDUCATION	UNIVERSITY OF MICHIGAN Stephen M. Ross School of Business Master of Business Administration, May 2007 <ul style="list-style-type: none">• Emphasis in New Business Development and Technology• Awarded merit-based Samuel Zell Scholarship in Entrepreneurial Studies• Selected to serve on Frankel Commercialization Fund, focused on pre-seed investments• Candidate for graduation with High Distinction; GMAT 710, 96th percentile	Ann Arbor, MI
	UNIVERSITY OF WASHINGTON Master of Science in Electrical Engineering, June 2001 <ul style="list-style-type: none">• Research Assistant, Adaptive Computing Machines and Emulators Lab• Completed NASA-sponsored research on image compression algorithms altered for satellite-based reconfigurable platforms yielding over a 1000% performance increase	Seattle, WA
	NORTHWESTERN UNIVERSITY Bachelor of Science in Computer Engineering, June 1998 <ul style="list-style-type: none">• Led two-year graduate level research project to design and integrate FPGA technology into a general purpose processor; project published and spawned multiple research initiatives at Northwestern University and the University of Washington	Evanston, IL
EXPERIENCE	TECHNOLOGY TRANSFER OFFICE, UNIV. OF MICHIGAN New Business Development Consultant <ul style="list-style-type: none">• Led evaluation of early-stage university research for commercialization potential, accelerating the business development of three university spin-outs.• Managed team of five associates in conducting market research and assessing market potential; significantly refocused target market for two pre-clinical biotech firms.	Ann Arbor, MI
Summer 2006		
2001-2005	IBM MICROELECTRONICS Staff Engineer/Scientist <ul style="list-style-type: none">• Led team responsible for clock distribution methodology in ASIC semiconductors, dramatically improved performance and turn-around time over a four-year period.• Identified unique opportunity to coordinate semiconductor research between multiple divisions; built management consensus to lead cross-divisional project leveraging clock design advances yielding a multi-year lead over IBM's competition.• Managed customer relationships by coordinating design efforts between departments; streamlined communication and significantly improved customer satisfaction.• Analyzed product requirements for high-performance semiconductors generating \$1B in annual revenues; developed new transistor placement and wiring algorithms resulting in a 300% performance improvement and a 50% design-time reduction.• Authored two patent applications after analyzing new low-power voltage domain semiconductor technology and addressing future design requirements.	Waltham, MA
1998-1999	UBS Software Developer <ul style="list-style-type: none">• Selected to perform independent software consulting services in 2000.• Led team that converted the HR systems from Sybase to the Oracle platform, completed initiative in half the projected time with half the budgeted resources.	Stamford, CT
1996-1999	KMF DEVELOPMENT Entrepreneur <ul style="list-style-type: none">• Founded KMF Development, an Internet solutions company, to assist corporations develop an on-line presence prior to the internet becoming mainstream.• Secured client base and formed new business relationships through interactions with senior client management. Educated management on the benefits of an on-line presence through demonstrations. Developed customer solutions, strategy and web site design.	Evanston, IL
ADDITIONAL	<ul style="list-style-type: none">• US Sailing certifications in Basic Keelboat, Basic Cruising and Coastal Navigation• Enjoy travel and have visited 4 continents and 48 states	

JOURNAL ARTICLES

- T. Fry, S. Hauck, "SPIHT Image Compression on FPGAs", *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 15, No. 9, pp. 1138-1147, September 2005.
- T. W. Fry, S. Hauck, M. M. Hosler, J. P. Kao, "The Chimaera Reconfigurable Functional Unit", *IEEE Transactions on VLSI Systems*, Vol. 12, No. 2, pp. 206-217, February 2004.
- S. Hauck, M. M. Hosler, T. W. Fry, "High-Performance Carry Chains in FPGAs", *IEEE Transactions on VLSI Systems*, Vol. 8, No. 2, pp. 138-147, April 2000.

PATENTS

- Fry, et al., *U.S. Patent No. 6,986,116*, "Signal Balancing Between Voltage Domains", Washington, DC: U.S. Patent and Trademark Office, awarded January 10, 2006.
- Fry, et al., *U.S. Patent No. 7,073,145*, "Programmable Delay Method for Hierarchical Signal Balancing", Washington, DC: U.S. Patent and Trademark Office, awarded July 4, 2006.

BOOK CHAPTERS

- T. W. Fry, "Chapter 6: Case Studies - Algorithm Alteration, Variable Precision, Image Compression: SPIHT Compression" in S. Hauck, A. DeHon, *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation*, in preparation for Morgan Kaufmann/Elsevier.

THESIS

- T. W. Fry, *Hyperspectral Image Compression on Reconfigurable Platforms*, M.S. Thesis, University of Washington, Department of Electrical Engineering, June 2001.

CONFERENCE PAPERS

- S. Hauck, T. W. Fry, M. M. Hosler, J. P. Kao, "The Chimaera Reconfigurable Functional Unit", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 87-96, 1997.
- S. Hauck, M. M. Hosler, T. W. Fry, "High-Performance Carry Chains for FPGAs", *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 223-233, 1998.
- T. W. Fry, S. Hauck, "Hyperspectral Image Compression on Reconfigurable Platforms", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 251-260, 2002.
- T. W. Fry, S. Hauck, "Image Compression on Reconfigurable Platforms", *Earth Science Technology Conference*, June, 2002.
- T. W. Fry, "ASIC Clock Methodology Direction", *IBM ASIC Specialty Training*, September 2002.
- T. W. Fry, "High-Performance Clock Grids in ASIC applications", *IBM ASIC Specialty Training*, November 2004.

TECHNICAL REPORTS

- T. W. Fry, "Live-Wire Boundary Detection of TRUS Prostate Images", *University of Washington, Dept. of EE*, Technical Report, 2000.